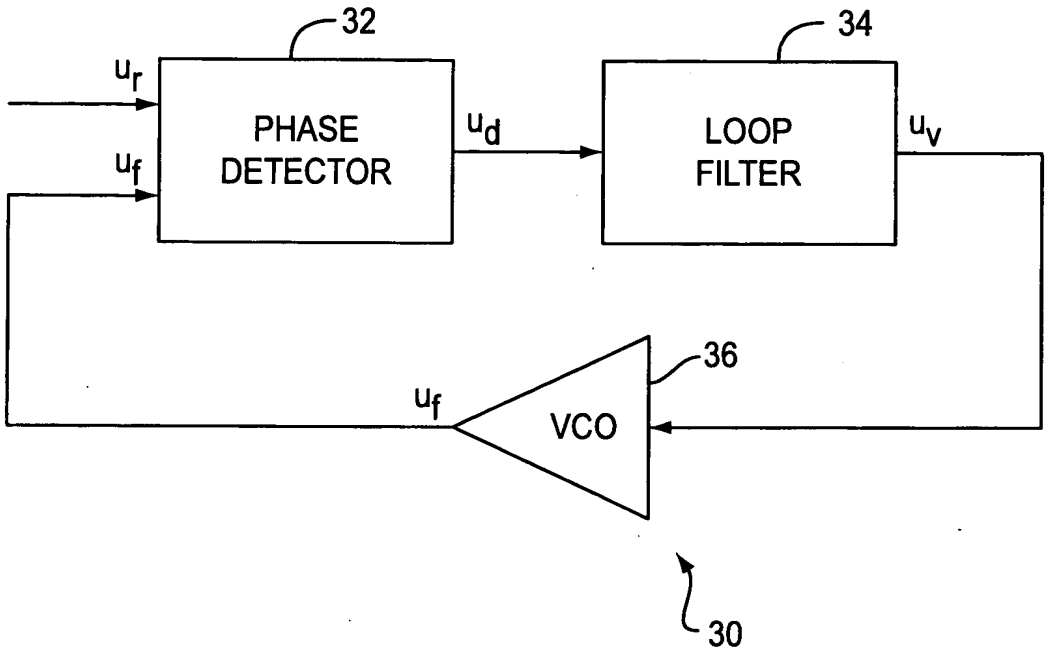

FIG. 1

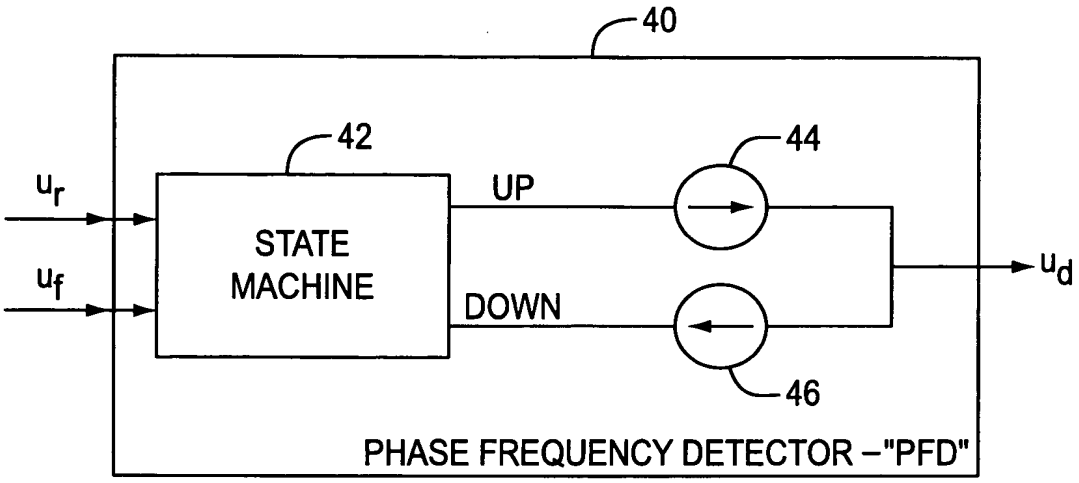
40
42
44
u_r
u_f
STATE MACHINE
UP
DOWN
u_d
46
PHASE FREQUENCY DETECTOR –"PFD"

FIG. 2

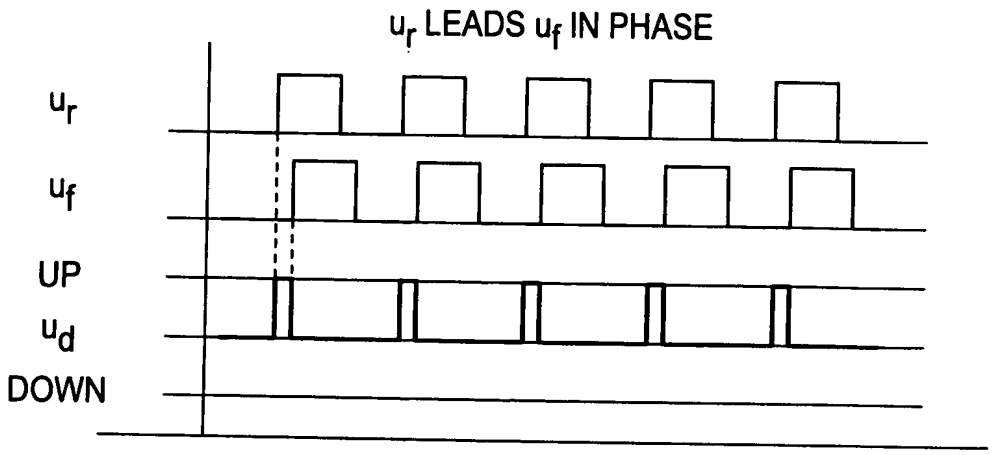

FIG. 3A

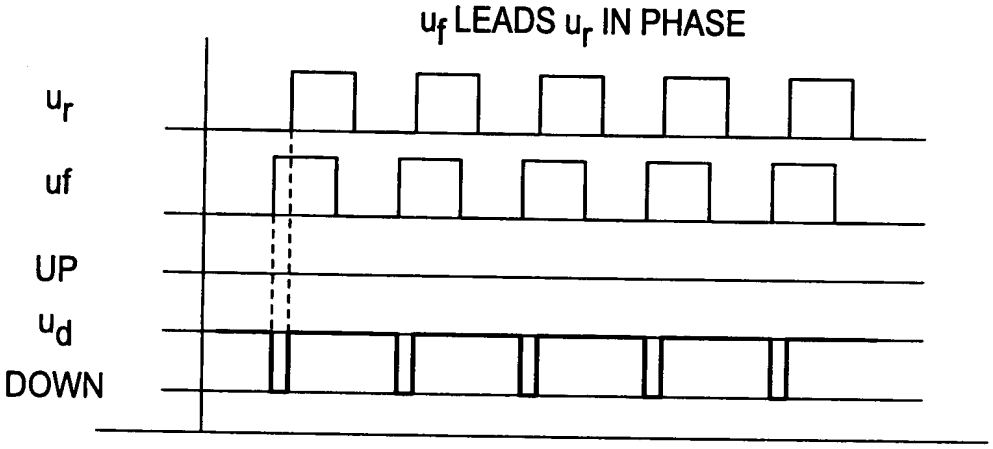

FIG. 3B

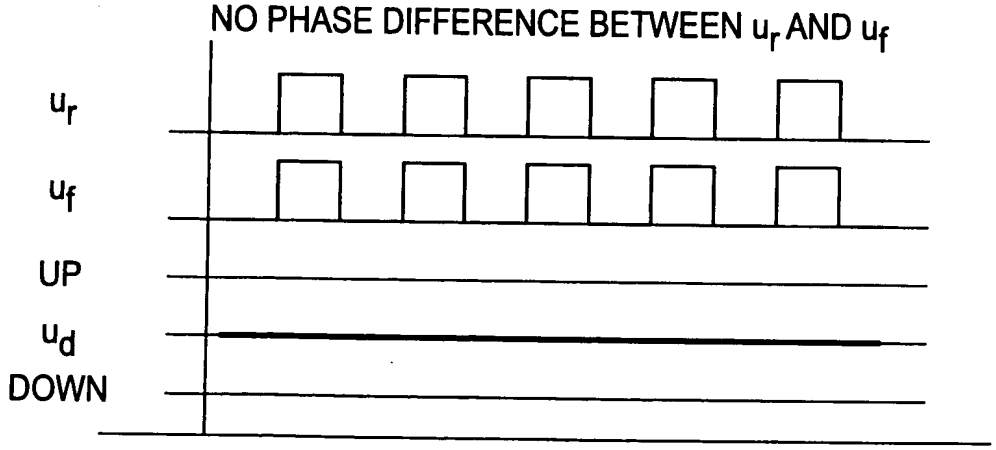

FIG. 3C

u_r - u_f	u_r - u_f	u_r - u_f	u_r - u_f	UP	DOWN
0-0	0-1	1-1	1-0		
(1)	2	2	(1)	0	1
3	(2)	(2)	6	0	1
(3)	4	5	6	1	1
8	(4)	5	7	1	1
3	2	(5)	7	1	1
1	2	5	(6)	1	1
3	4	(7)	(7)	1	0
(8)	(8)	7	7	1	0

PFD STATE TRANSITION TABLE

FIG. 4

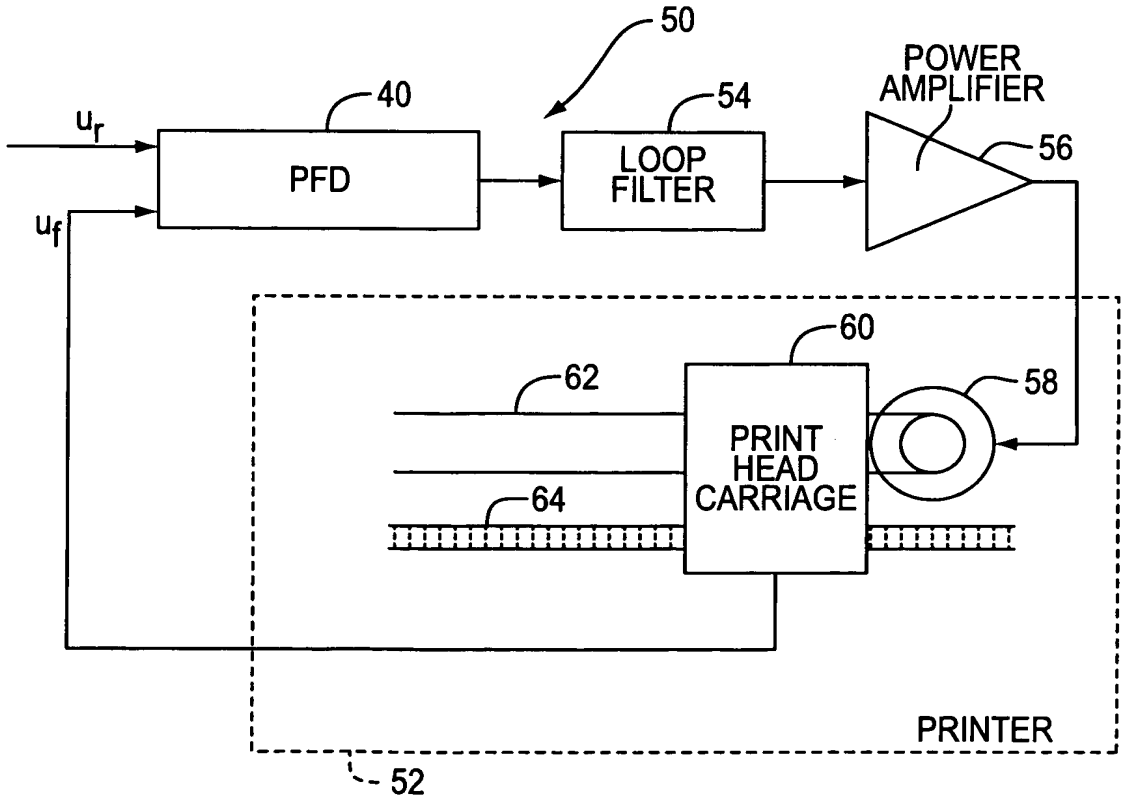

FIG. 5

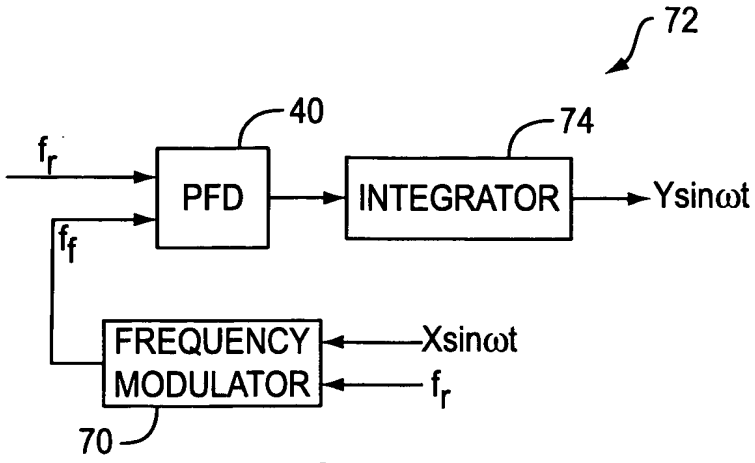
72
40
74
f_r
PFD
INTEGRATOR
Ysinωt
f_f
FREQUENCY
MODULATOR
Xsinωt
f_r
70

FIG. 6

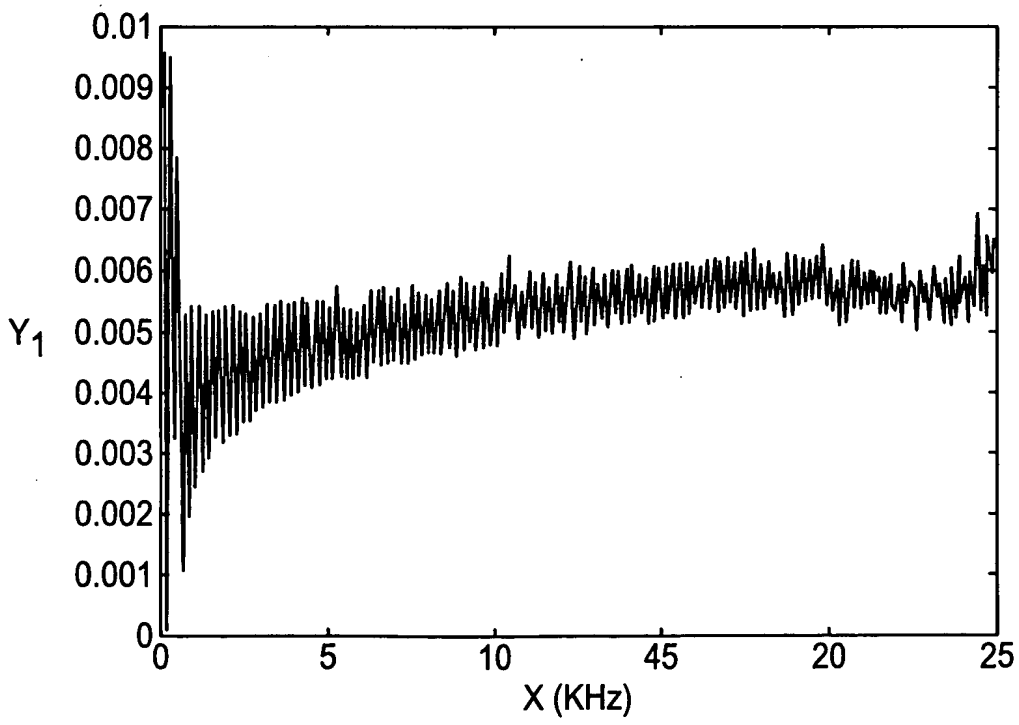
0.01
0.009
0.008
0.007
0.006
0.005
0.004
0.003
0.002
0.001
0
Y_1
0
5
10
45
20
25
X (KHz)

FIG. 8

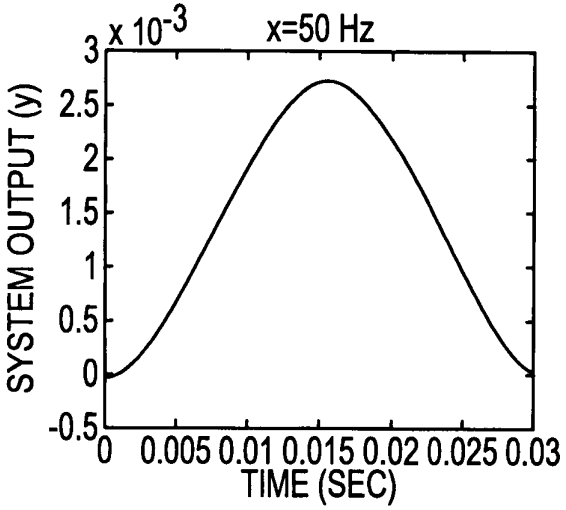

FIG. 7A

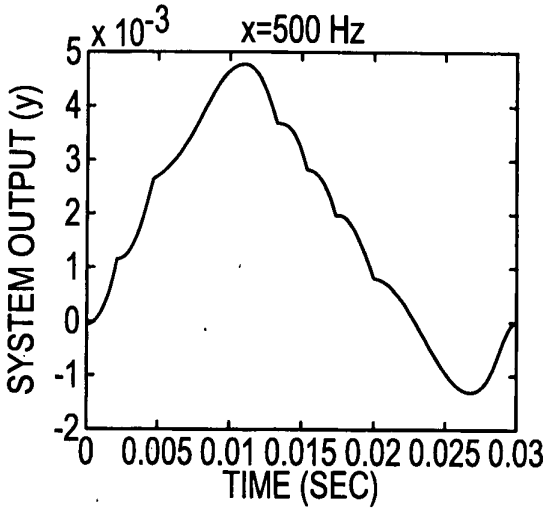

FIG. 7B

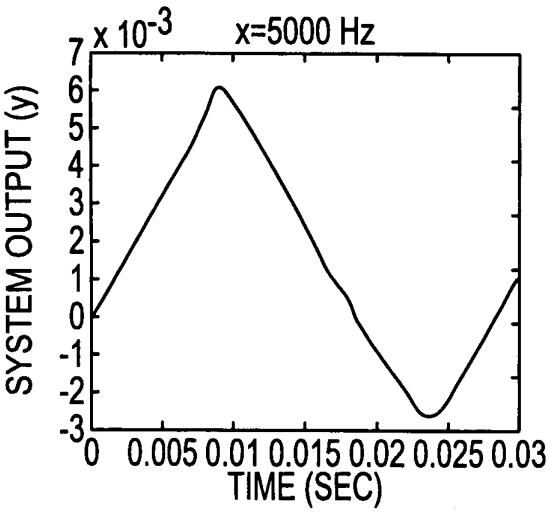

FIG. 7C

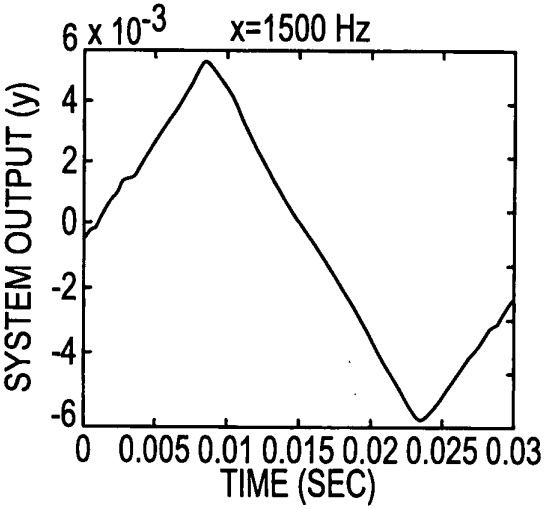

FIG. 7D

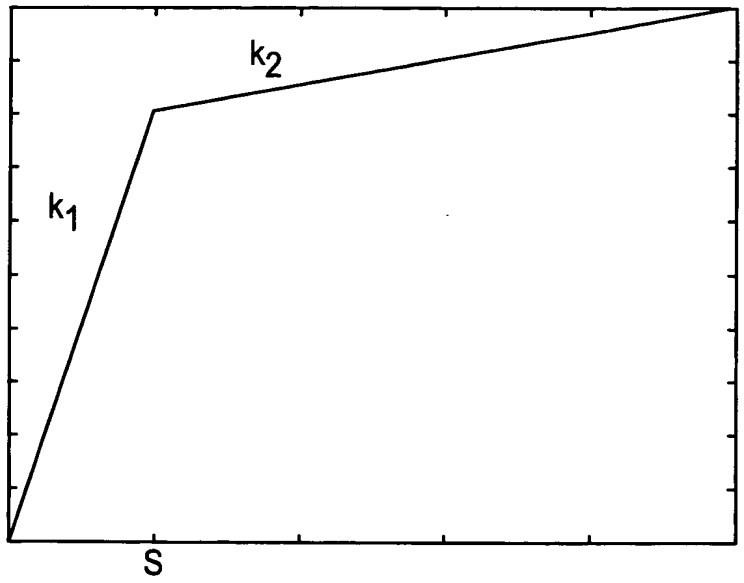
k2
k1
S

FIG. 9

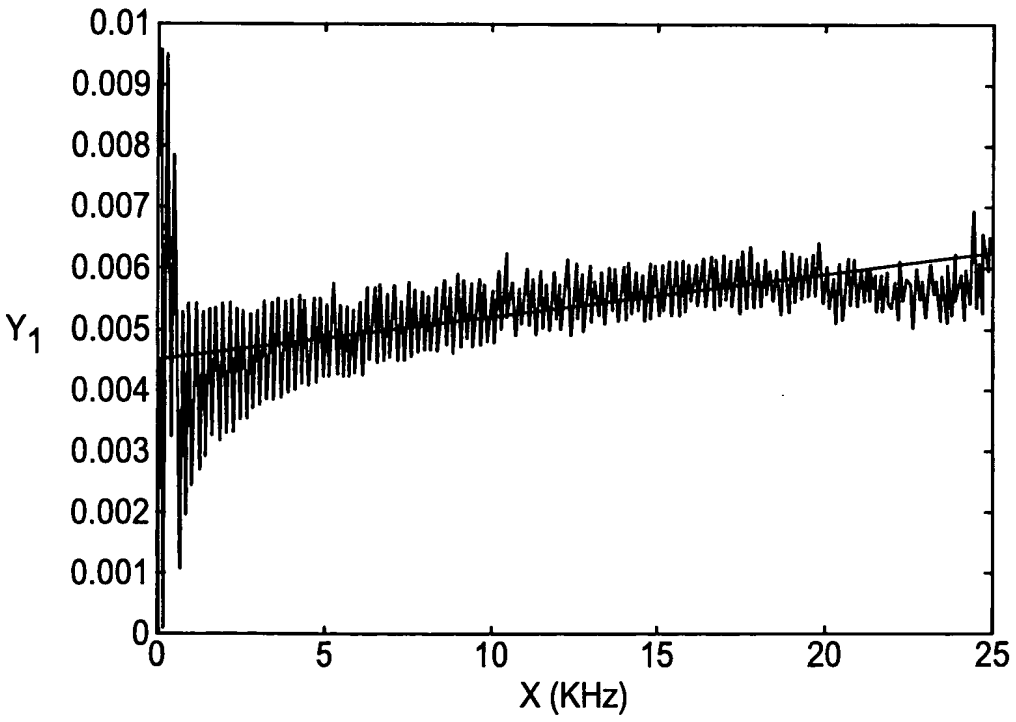
0.01
0.009
0.008
0.007
0.006
0.005
0.004
0.003
0.002
0.001
0
Y1
0
5
10
15
20
25
X (KHz)

FIG. 10

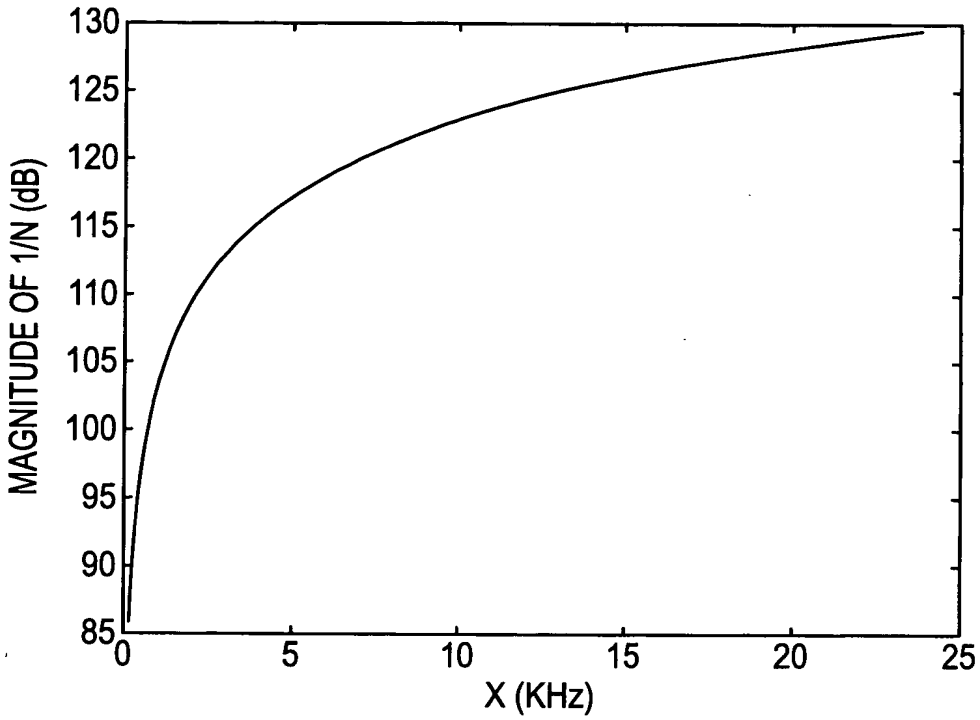
130
125
120
115
110
105
100
95
90
85
MAGNITUDE OF 1/N (dB)
0
5
10
15
20
25
X (KHz)

FIG. 11

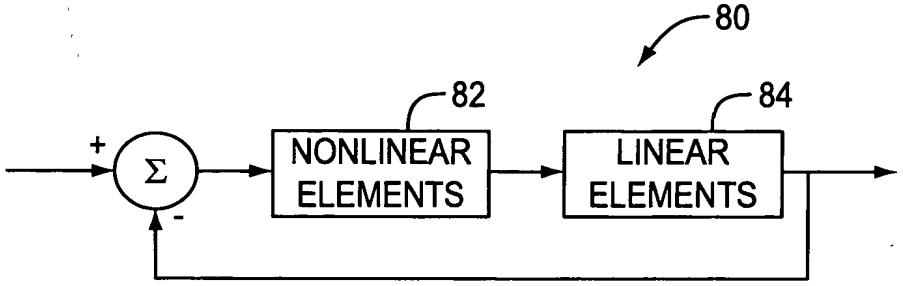
80
82
84
+
Σ
-
NONLINEAR ELEMENTS
LINEAR ELEMENTS

FIG. 12

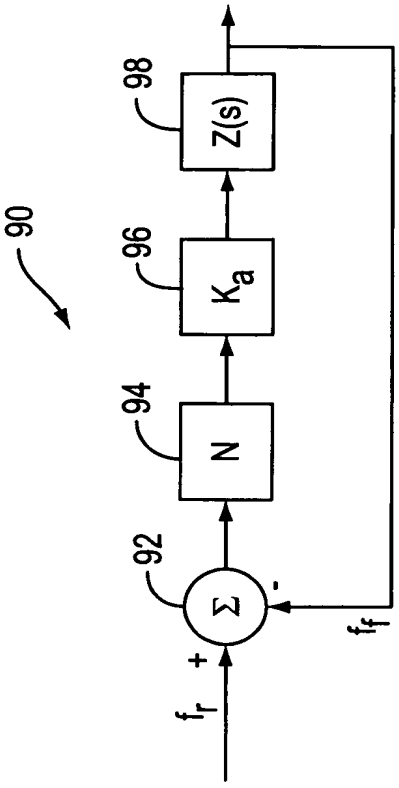
90
92
Σ
+
-
f_r
f_f
94
N
96
K_a
98
Z(s)

FIG. 13

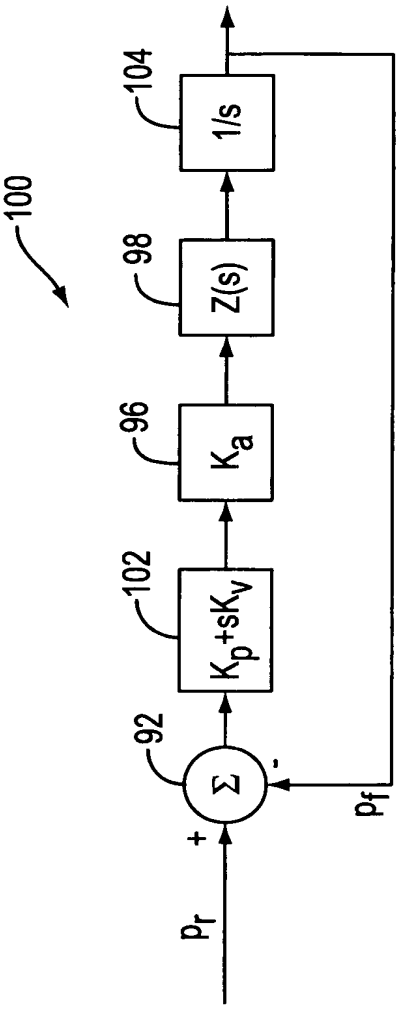
100
92
Σ
+
-
p_r
p_f
102
K_p+sK_v
96
K_a
98
Z(s)
104
1/s

FIG. 14

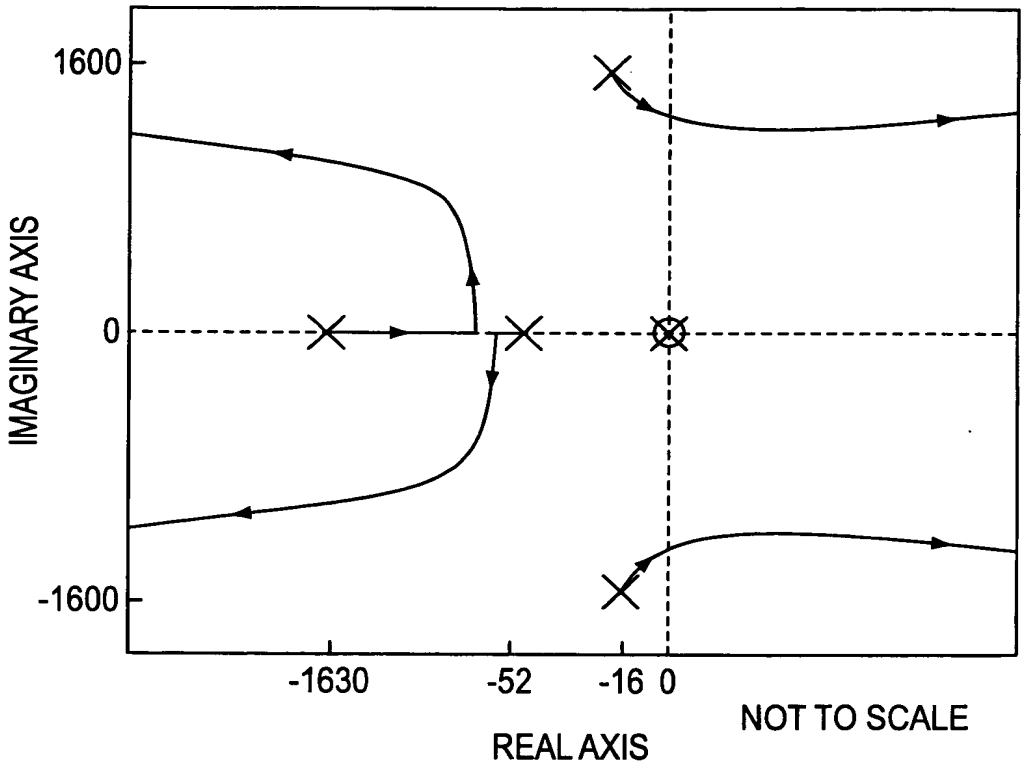

FIG. 15

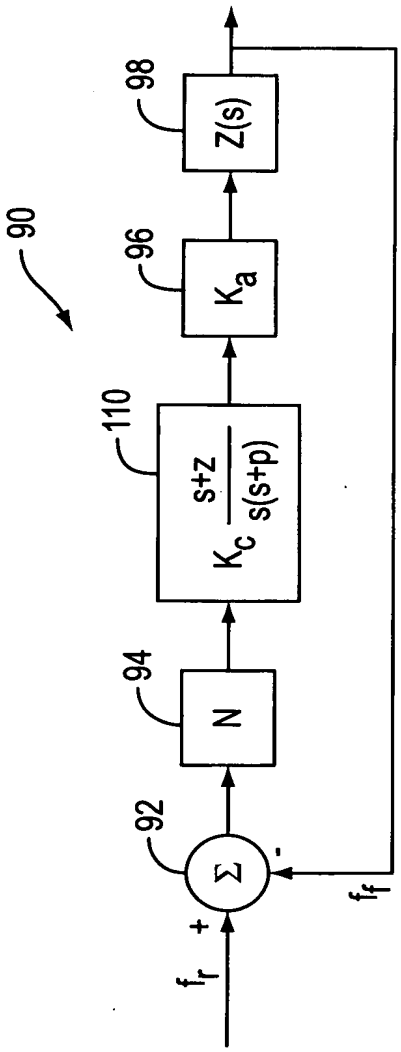
90
92
Σ
+
-
f_r
f_f
94
N
110
$K_c \frac{s+z}{s(s+p)}$
96
K_a
98
Z(s)

FIG. 16

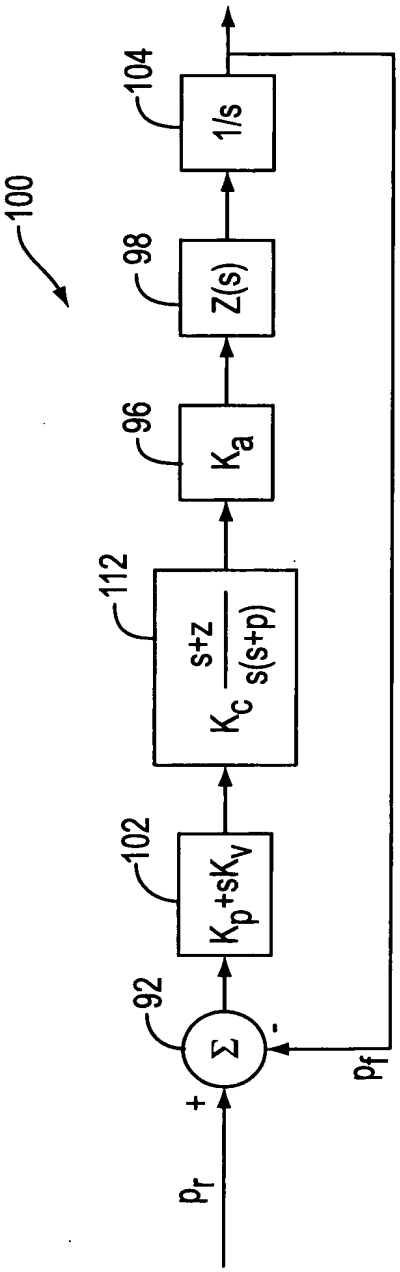
100
92
Σ
+
-
p_r
p_f
102
K_p+sK_V
112
$K_c \frac{s+z}{s(s+p)}$
96
K_a
98
Z(s)
104
1/s

FIG. 17

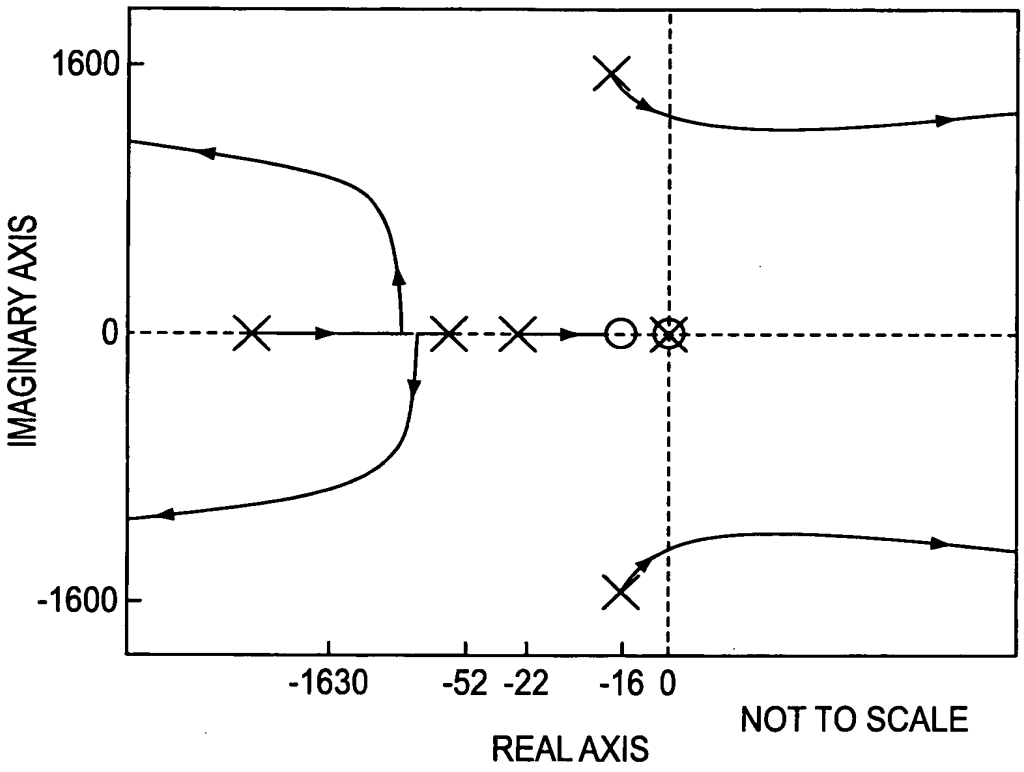
1600
0
-1600
IMAGINARY AXIS
-1630
-52
-22
-16
0
REAL AXIS
NOT TO SCALE

FIG. 18

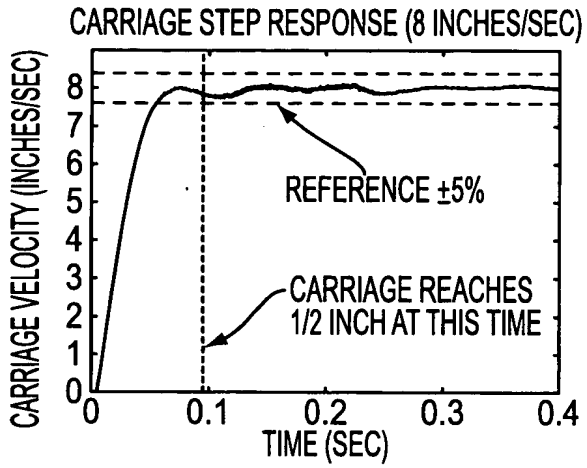

FIG. 19A

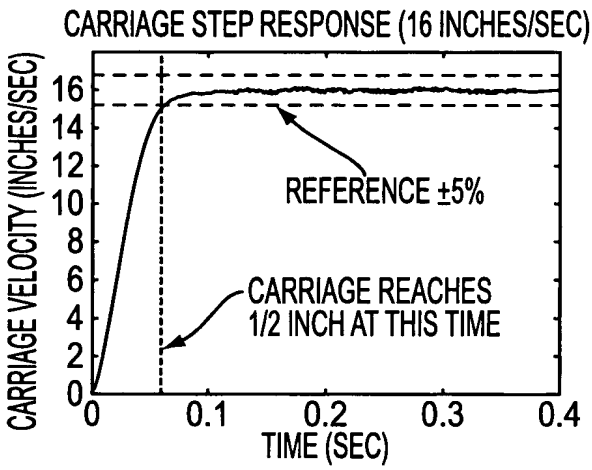

FIG. 19B

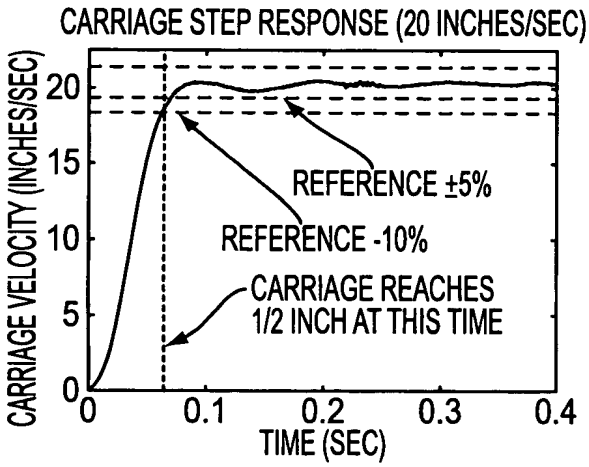

FIG. 19C

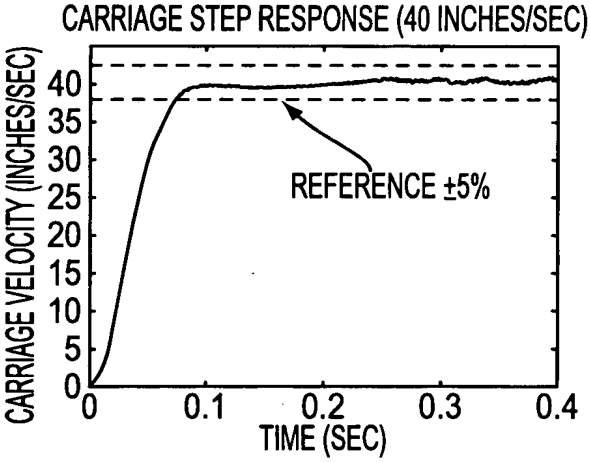

FIG. 19D

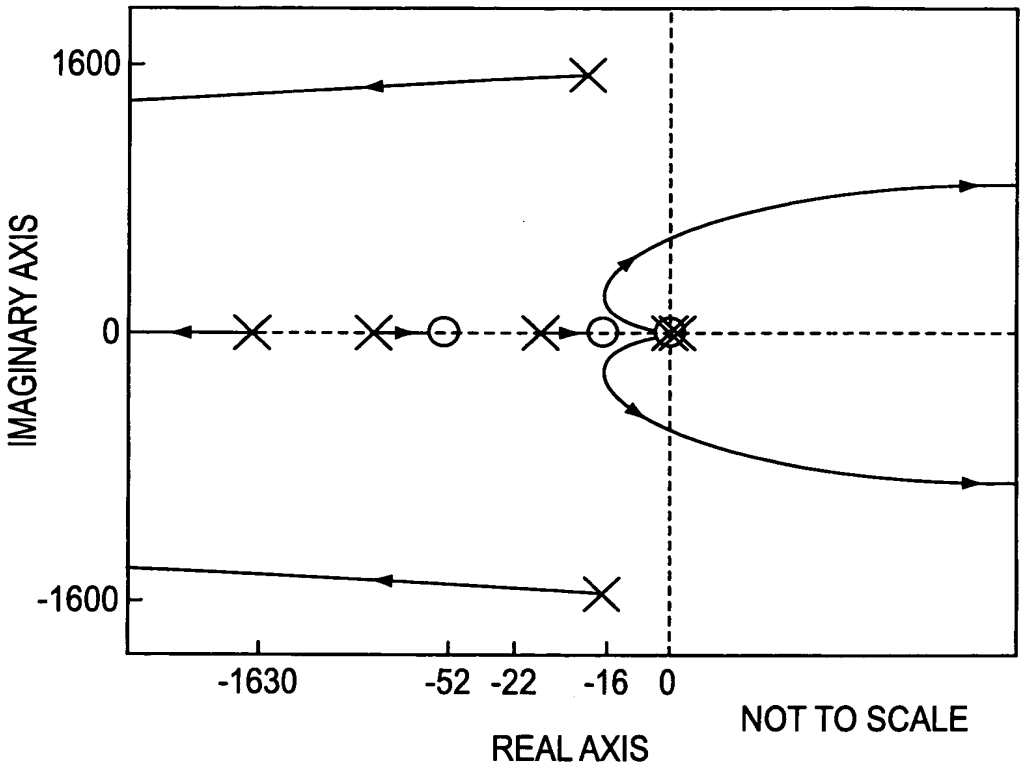
1600
0
-1600
IMAGINARY AXIS
-1630
-52
-22
-16
0
REAL AXIS
NOT TO SCALE

FIG. 20

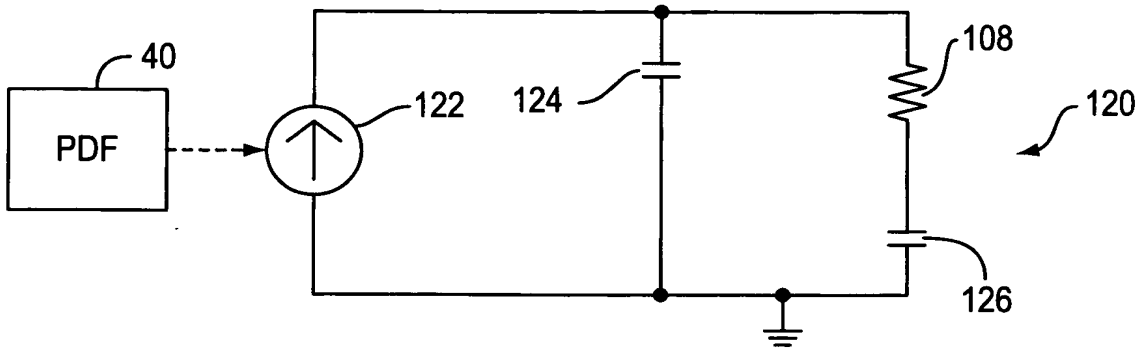
40
PDF
122
124
108
120
126

FIG. 21

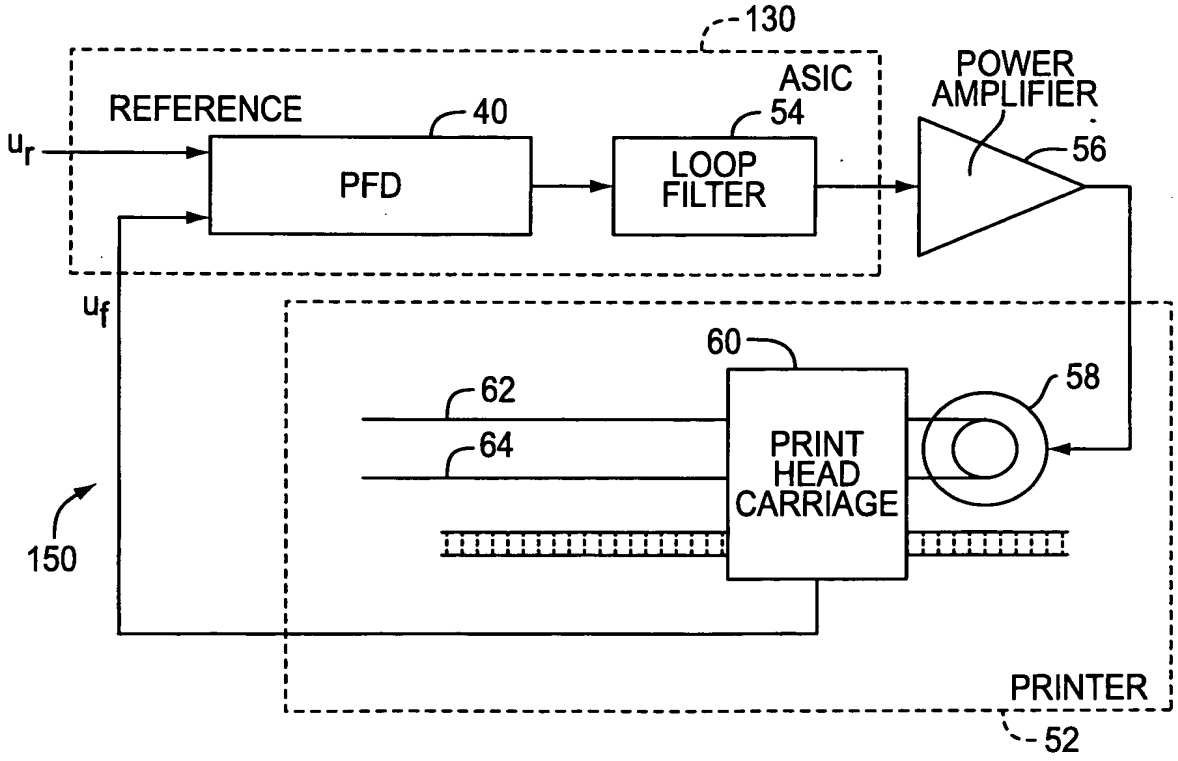
130
ASIC
REFERENCE
40
54
POWER
AMPLIFIER
u_r
PFD
LOOP
FILTER
56
u_f
60
62
58
64
PRINT
HEAD
CARRIAGE
150
PRINTER
52

FIG. 23

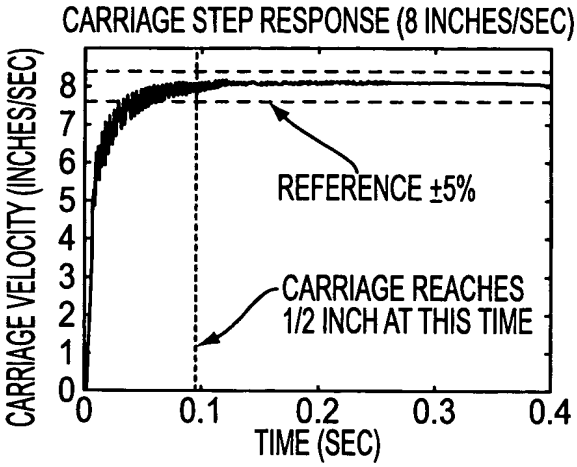

FIG. 24A

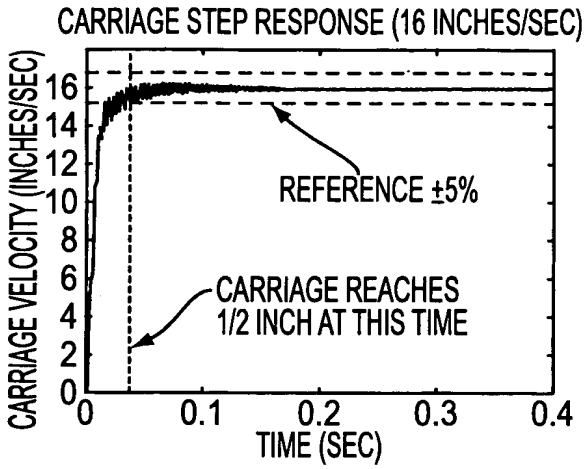

FIG. 24B

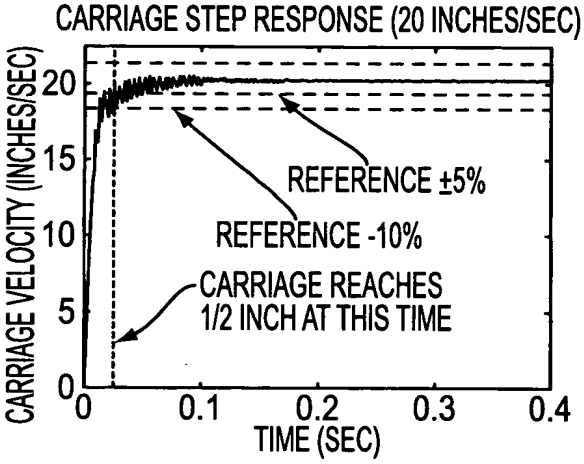

FIG. 24C

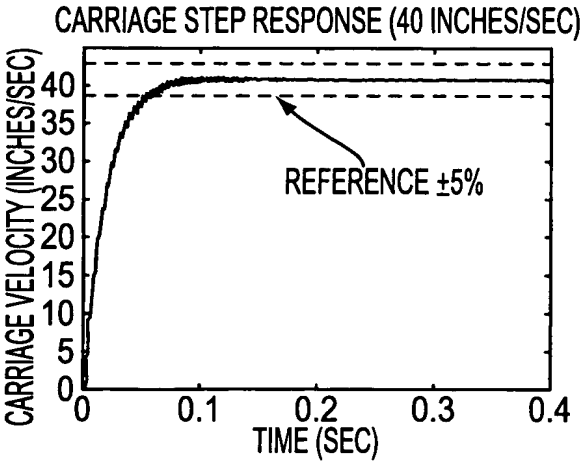

FIG. 24D

CAPACITOR VOLTAGES	PFD "UP"	PFD "DOWN"	PFD "OFF" Vc124>Vc126	PFD "ON" Vc124<Vc126
Vc124	INCREASES	DECREASES	DECREASES	INCREASES
Vc126	INCREASES	DECREASES	INCREASES	DECREASES

OPERATION OF ANALOG LOOP FILTER

FIG. 22

PRINT SPEED (ips)	PRELOAD ACCUMULATOR 1	PRELOAD ACCUMULATOR 2	FREQUENCY (Hz) ACCUMULATOR 1	FREQUENCY (Hz) ACCUMULATOR 2
8	500	290	50,000	100
16	800	300	50,000	100
20	900	350	50,000	100
40	900	650	50,000	100

DESIGN PARAMETERS OF ADPLL FOR VARIOUS PRINT SPEEDS

FIG. 25

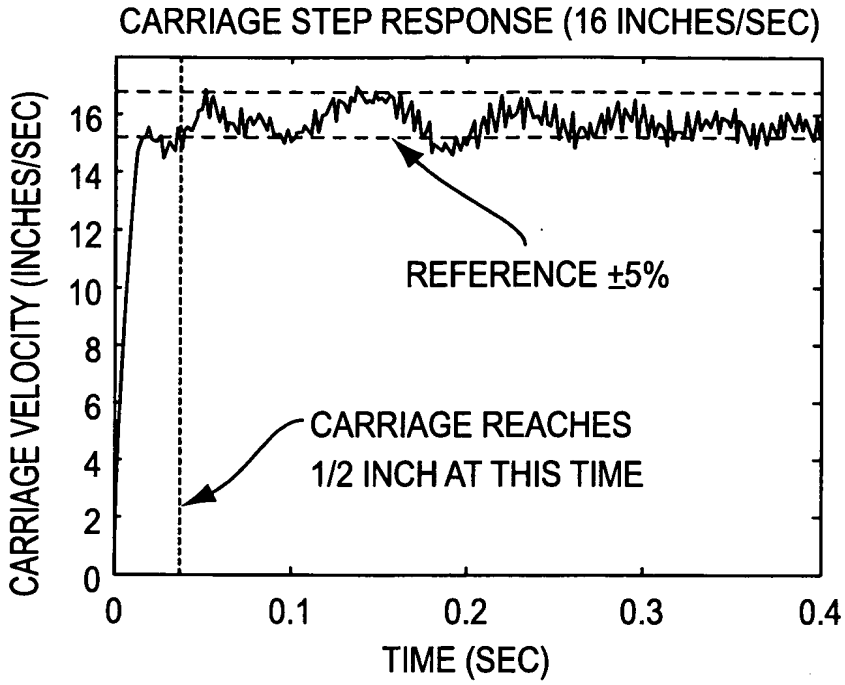
CARRIAGE STEP RESPONSE (16 INCHES/SEC)
CARRIAGE VELOCITY (INCHES/SEC)
16
14
12
10
8
6
4
2
0
REFERENCE ±5%
CARRIAGE REACHES
1/2 INCH AT THIS TIME
0
0.1
0.2
0.3
0.4
TIME (SEC)

FIG. 26

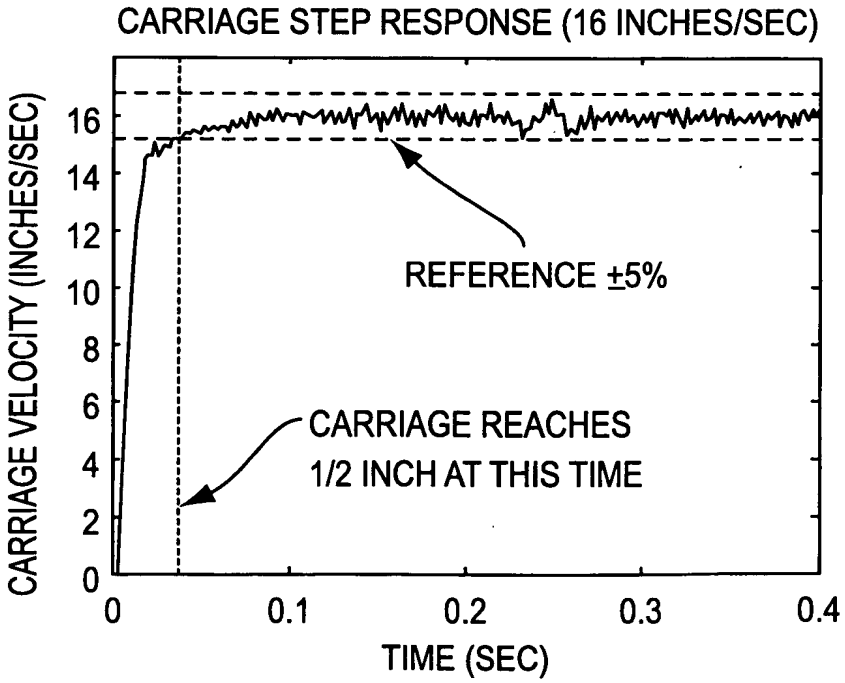
CARRIAGE STEP RESPONSE (16 INCHES/SEC)
CARRIAGE VELOCITY (INCHES/SEC)
16
14
12
10
8
6
4
2
0
REFERENCE ±5%
CARRIAGE REACHES
1/2 INCH AT THIS TIME
0
0.1
0.2
0.3
0.4
TIME (SEC)

FIG. 28

u_r-u_f	u_r-u_f	u_r-u_f	u_r-u_f	UP	DOWN
0-0	0-1	1-1	1-0		
(1)	2	2	(1)	1	1
4	(2)	(2)	7	1	1
4	(3)	2	7	0	1
(4)	5	6	7	1	1
8	(5)	6	9	1	1
4	3	(6)	9	1	1
1	3	6	(7)	1	1
(8)	10	10	(8)	1	1
4	5	10	(9)	1	0
4	5	(10)	(10)	1	1

PFD STATE TRANSITION TABLE

FIG. 27